Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-18. (cancelled)

19. (new) A variable gain amplifier, comprising:

a first transistor and a second transistor coupled together differentially;

a plurality of degeneration resistance circuits, each having a switch responsive to a control voltage, coupled to said first transistor and said second transistor; and

means for varying the control voltage to stagger turn-on of said plurality of degeneration resistance circuits.

20. (new) The amplifier of claim 20, wherein each of said plurality of degeneration resistance circuits has an approximately equal resistance.

21. (new) The amplifier of claim 20, wherein each of said plurality of degeneration resistance circuits has a resistance, said resistance of a first degeneration resistance circuit being greater than said resistance of a second degeneration resistance circuit.

22. (new) The amplifier of claim 20, wherein said means for varying the control voltage includes a voltage offset ladder circuit.

23. (new) The amplifier of claim 20, wherein said first transistor and said second transistor are NMOS devices.

24. (new) An integrated circuit, comprising:

a substrate; and

a variable gain amplifier, disposed on said substrate, including

a first transistor and a second transistor coupled together differentially,

a plurality of degeneration resistance circuits, each having a switch responsive to a voltage, coupled to said first transistor and said second transistor, and

a control circuit that varies the voltage to stagger turn-on of said plurality of degeneration resistance circuits.

25. (new) The integrated circuit of claim 24, further comprising:

a receiver, disposed on said substrate, that converts a received RF signal to an IF signal, and

wherein said variable gain amplifier amplifies the IF signal.

26. (new) The integrated circuit of claim 25, wherein the gain of said variable gain amplifier is responsive to a strength of the RF signal.

27. (new) The integrated circuit of claim 25, wherein each of said plurality of degeneration resistance circuits has an approximately equal resistance.

28. (new) The integrated circuit of claim 25, wherein each of said plurality of degeneration resistance circuits has a resistance, said resistance of a first degeneration resistance circuit being greater than said resistance of a second degeneration resistance circuit.

29. (new) The integrated circuit of claim 25, wherein said control circuit includes a voltage offset ladder circuit.

30. (new) The integrated circuit of claim 25, wherein said first transistor and said second transistor are NMOS devices.

31. (new) A system for amplifying a signal, comprising:

a first transistor and a second transistor coupled together differentially,

a plurality of degeneration resistance circuits, each having a switch responsive to a first voltage, coupled to said first transistor and said second transistor; and

a control circuit that varies the first voltage to stagger turn-on of said plurality of degeneration resistance circuits.

32. (new) The system of claim 31, wherein the amplification of an input signal is proportional to a strength of the input signal.

33. (new) The system of claim 31, wherein the amplification of an input signal is proportional to a strength of a second signal.

34. (new) The system of claim 33, wherein the input signal is derived from the second signal.

35. (new) The system of claim 31, wherein each of said plurality of degeneration resistance circuits has an approximately equal resistance.

36. (new) The system of claim 31, wherein each of said plurality of degeneration resistance circuits has a resistance, said resistance of a first degeneration resistance circuit being greater than said resistance of a second degeneration resistance circuit.

37. (new) The system of claim 31, wherein said control circuit includes a voltage offset ladder circuit.

38. (new) The system of claim 31, wherein said first transistor and said second transistor are NMOS devices.